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10/596,573	10/14/2008	Zhong-Xiang He	BUR920030081US1	7999

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EXAMINER	
SENGDARA, VONGSAVANH	
ART UNIT	**PAPER NUMBER**
2826	

NOTIFICATION DATE	DELIVERY MODE
05/29/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

EFIPLAW@US.IBM.COM

Office Action Summary	Application No.	Applicant(s)	
	10/596,573	HE ET AL.	
	Examiner	Art Unit	
	VONGSAVANH SENGDARA	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 June 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/15/2007, 01/15/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings Objection

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, regarding the limitations of the claims enumerated below

claim 1 - lines 6 - 7;

claim 2 – line 2 (“the first second contact in said wiring layer")

claim 4 - lines 1 - 2;

claim 5 – lines 1 – 2;

claim 8 – lines 1 - 4;

must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Referring to fig. 1 and fig. 6 of Applicant drawings, fig. 1and fig. 6 disclose that the NPN device (the tallest device) is in direct contact with the CE and the CE is in contact with the wiring layer. Examiner interprets that the Applicant claimed invention to mean the CE is a part of the NPN transistor and therefore the NPN device as interpreted is in a direct contact with the wiring layer.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure

is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification Objection

Claims 1-11 are objected to because of the following informalities: the Applicant specification does not disclose of (a) "first contact' and (b) second contact. Appropriate correction is required.

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: the Applicant specification does not disclose of (a) "first contact' and (b) "second contact".

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 1 – lines 6—7, the limitation of

> "wherein at least one of the tallest of said plurality of devices is in direct contact with said wiring layer"

is unclear as to whether the Applicant considers the"contact emitter" to be a part of the NPN transistor. Examiner interprets that the Applicant claimed invention to mean the CE is a part of the NPN transistor and therefore the NPN device as interpreted is in a direct contact with the wiring layer. Otherwise, it is unclear as to how the NPN transistor can be in direct contact with the wiring layer since it is "contact emitter" which is in direct contact with the wiring layer as illustrated in fig. 1 and fig. 6 of the Applicant's drawing.

Regarding claim 2, it is unclear as to what is a "first second contact". It is unclear as to how a contact can be both a first contact as well as a second. Furthermore, it is unclear as to how the "tallest device", which is the NPN transistor in fig. 1 and fig. 6 of the Applicant's drawing, can be in direct contact with the "first second contact" since fig. 1 and fig. 6 of the Applicant's drawing illustrates that the NPN transistor is in direct contact with the "contact emitter". Examiner will consider Applicant's "first second contact" to the contact which the examiner labeled "A" in fig. 1 of Ohnishi et al.

Regarding claim 3, Claim 3 recites the limitation “said second contact" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Regarding claim 4, it is unclear as to how “said second contact extends through said wiring layer to said via layer” since the Applicant's drawing illustrates that it is the contact which extends through the via layer to the wiring layer – note the examiner will interpret the Applicant's claimed invention to me a contact which extends through the via layer to the wiring layer.

Regarding claim 5, it is unclear as to how “said second contact is positioned within said wiring layer” since the Applicant's drawing illustrates that it is second contact that is positioned within said via layer – note the examiner will interpret the Applicant's claimed invention to mean that it is the second contact that is positioned within said via layer.

Regarding claim 8, it is unclear as what the Applicant is referring to as "a first second contact" furthermore, Applicant drawing only shows the wiring within the wiring layer therefore examiner is unclear as to what the applicant is exactly trying to convey by "wherein said at least one of the tallest of said plurality of devices is in direct contact with a first second contact in said wiring layer” because only wire is shown to exist in Applicant's drawing - therefore, examiner will interpret that this limitation to mean "wherein said at least one of the tallest of said plurality of devices is in direct contact with a wire in said wiring layer”. In addition, examiner is unclear as to what the Applicant is trying to convey by the limitation “said second contact within said wiring layer comprises a different material than said wiring within said wiring layer” because second

contact is within said via layer above the said wiring layer – therefore, examiner will interpret this limitation to mean "said second contact within said vai layer comprises a different material than said wiring within said wiring layer".

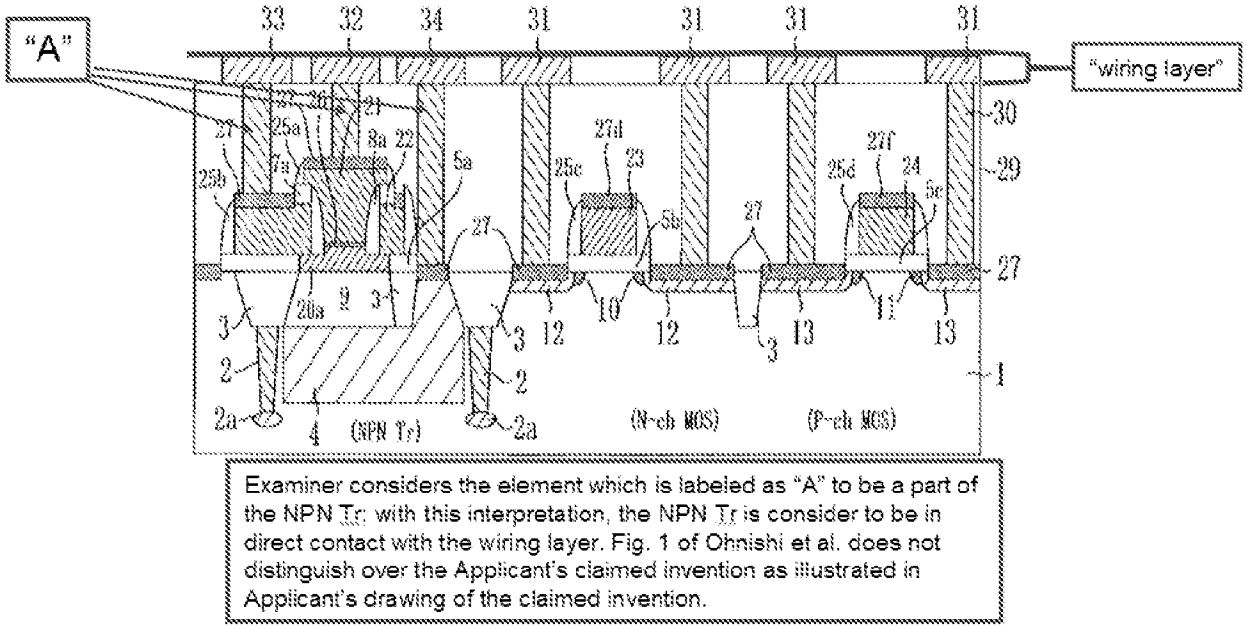
Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 6, 7, 9, 10, 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Ohnishi et al. (6399993).

FIG. 1



Regarding claims 1 and 12, fig. 1 of Ohnishi et al. discloses an integrated circuit structure comprising:

a substrate 1;

a plurality of different height devices (three total: (1) NPN Tr, (2) N-ch MOS, and (3) P-ch MOS) positioned on said substrate 1;

a passivating layer 29 positioned above said substrate 1 and between said devices;

a wiring layer (examiner labeled as "wiring layer") above said passivating layer 1, wherein at least one of the tallest (NPN Tr) of said plurality of devices is in direct contact with said wiring layer and at least one of the shorter (N-ch MOS or P-ch MOS) of said plurality of devices is connected

to said wiring layer by a first contact 30 extending through said passivating layer 29.

NOTE: Examiner considers the element which is labeled as "A" to be a part of the NPN Tr; with this interpretation, the NPN Tr is consider to be in direct contact with the wiring layer. Fig. 1 of Ohnishi et al. does not distinguish over the Applicant's claimed invention as illustrated in Applicant's drawing of the claimed invention.

Note: the method of forming as recited in claim 12 does not recite any specific process step and the general process steps such as forming and removing as recited in the claim 12 would have been inherent in order to form the integrated structure of claim 1, and therefore claim 12 is consider to be inherently disclosed by fig. 1 of Ohnishi et al.

Regarding claim 2, with reference to 112 2nd rejection, fig 1 of Ohnishi et al. further discloses wherein said at least one of the tallest of said plurality of devices is in direct contact with a first second contact (examiner interpret this be the contact "A" which the examiner labeled in fig. 1 of Ohnishi et al. above) in said wiring layer.

Regarding claim 6, fig 1 of Ohnishi et al. further discloses wherein said wiring layer further comprises wiring (31, 32, 33, 34) within said wiring layer.

Regarding claim 7, fig 1 of Ohnishi et al. further discloses said first contact 30 is connected to said wiring 31 in said wiring layer.

Regarding claim 9, fig 1 of Ohnishi et al. further discloses wherein said at least one of the tallest of said plurality of devices (NPN Tr) comprises a different type of device (NPN Tr) than said at least one of the shorter (MOSFETs) of said plurality of devices.

Regarding 10, with reference to 112 2nd rejection, fig 1 of Ohnishi et al. further disclose wherein the top of said at least one of the tallest (which the examiner interpret to be the top of element "A" as labeled in fig. 1) of said plurality of devices is substantially coplanar (the top of "A" is coplanar) with the top of said passivating layer 29.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohnishi et al. (6399993).

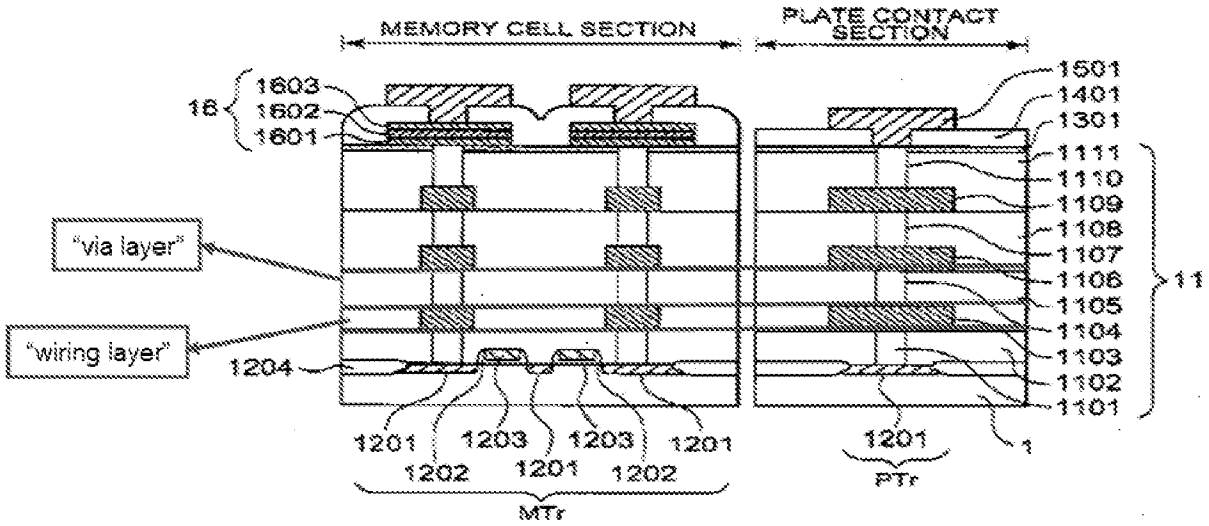
Regarding claim 11, Ohnishi et al. discloses all the limitation 10. Ohnishi et al. do not disclose wherein the top of said passivating layer is at a height, which the examiner considers to be a result effective variable and the examiner calls this distance – "The Distance", within about 50 nanometers from the top of said at least one of the tallest of said plurality of devices.

However, the optimization of "The Distance" would have been necessary to accommodate shrinking geometry in order to minimize cost. Therefore, the claims are obvious without showing that the claimed range(s) achieve unexpected results relative to the prior art range. *In re Woodruff*, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also *In re Huang*, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996) (claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also *In re Boesch*, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and *In re Aller*, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).

Claims 3, 4, 5, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohnishi et al. (6399993) in view of Mori (2004/0021222).

Regarding claim 3, Ohnishi et al. discloses all the limitations of claim 2. Ohnishi et al. does not disclose further comprising a via layer above said wiring layer, wherein said second contact is directly connected to said via layer.

FIG. 15



However, fig. 15 of Mori disclose a discloses an integrated circuit structure comprising: a substrate 1; a plurality of devices positioned on said substrate 1; a passivating layer 1102 positioned above said substrate 1 and between said devices; a wiring layer (examiner labeled as “wiring layer”) above said passivating layer 1.

Fig. 1 of Mori further discloses comprising a via layer (examiner labeled as “via layer”) above said wiring layer, wherein said second contact 1104 is directly connected to said via layer.

In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to for an integrated circuit structure of

Ohnishi et al.that further comprises a via layer above said wiring layer, wherein said second contact is directly connected to said via layer such as taught by Mori in order to form interconnect structure necessary to interconnect the plurality of devices to other circuit elements.

Regarding claim 4, with reference to 112 2nd rejection, fig. 15 of Mori further disclose wherein said second contact extends through said via layer to said wiring layer.

In view of such teaching it would have been obvious to one of ordinary skill in the art at the time the invention was made of an integrated circuit structure of Ohnishi et al. and Mori wherein said second contact extends through said via layer to said wiring layer such as taught by Mori in order to be able to make interconnection to the different wiring layers.

Regarding claim 5, with reference to 112 2nd rejection, fig. 15 of Mori further disclose wherein said second contact is positioned within said via layer.

In view of such teaching it would have been obvious to one of ordinary skill in the art at the time the invention was made of an integrated circuit structure of Ohnishi et al. and Mori wherein said second contact is positioned within said via layer such as taught by Mori in order to form an interconnection path to make interconnection to the different wiring layers.

Regarding claim 8, with reference to 112 2nd rejection, fig. 15 of Mori further discloses where said at least one of the tallest of said plurality of devices is in direct contact with a wire in said wiring layer (made of aluminum- see par [0074]) and said

second contact (Tungsten - see par [0068]) within said via layer comprises a different material than said wiring within said wiring layer.

In view of such teaching it would have been obvious to one of ordinary skill in the art at the time the invention was made of an integrated circuit structure of Ohnishi et al. and Mori where said at least one of the tallest of said plurality of devices is in direct contact with a wire in said wiring layer and said second contact within said via layer comprises a different material than said wiring within said wiring layer such as taught by Mori as it is convention to use Tungsten as a contact plug and aluminum as a wire in order to ensure profitable device functioning.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to VONGSAVANH SENGDARA whose telephone number is (571)270-5770. The examiner can normally be reached on flex schedule.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571)272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/V. S./
Examiner, Art Unit 2826

/Minh-Loan T. Tran/
Primary Examiner
Art Unit 2826